## AMENDMENTS TO THE CLAIMS

**This listing of claims will replace all prior versions and listings of claims in the application:**

**LISTING OF CLAIMS:**

1. (currently amended): A method of testing the operation of an electronic unit by stimulating said unit with simulated input signals to said unit, the method comprising:

- sending simulated input signals to said unit and receiving slow output signals from said unit in response to said simulated input ~~simulation~~ signals by at least one microprocessor;

- receiving fast output signals in response to said simulated input ~~simulation~~ signals by at least one programmable logic circuit; and

- processing the fast output signals by the at least one logic circuit to generate parameter values at a first frequency;

- storing said parameter values corresponding to said processed signals in a storing circuit; and

- accessing said stored parameter values by the at least one microprocessor at a second frequency which is slower than said first frequency and is compatible with an operating frequency of the microprocessor that generates said simulated input signals.

2. (currently amended): A method according to claim 1, wherein said parameter values are representative of switching instants of ~~logic signals generated by said unit~~said fast output signals.

3. (original): A method according to claim 2, wherein said parameter values are an image of said switching instants, of the duration during which a logic variable has a

predetermined value, and/or the mean value of a logic variable over a predetermined period.

4. (canceled).

5. (currently amended): An apparatus for testing the operation of an electronic unit by simulation, said unit generating logic signals at specific instants, said apparatus comprising a simulator which comprises:

- at least one microprocessor sending simulated input ~~simulation~~ signals to said unit and receiving slow output signals from said unit in response to said simulated input ~~simulation~~ signals;

- at least one programmable logic circuit which receives at least one of fast output signals from said unit, said logic circuit processing the fast output signals to generate, at a first frequency, parameter values corresponding to the fast output signals; and

- a storing circuit which stores said parameter values, wherein said microprocessor accesses said stored parameter values at a second frequency which is slower than said first frequency and is compatible with an operating frequency of said microprocessor.

6. (previously presented): An apparatus according to claim 5 further comprising at least one second programmable logic circuit which sends in real time simulation signals to said unit on the basis of reference signals previously issued by said microprocessor.

7. (previously presented): An apparatus according to claim 6, wherein said programmable logic circuit which receives said at least one of said fast output signals and said second programmable logic circuit which sends simulation signals to said unit are implemented as a single electronic circuit.

8. (currently amended): ~~An~~ The apparatus according to claim ~~5~~6, wherein said at least

one ~~of said~~ programmable logic circuit and said at least one second programmable logic circuit is of the field programmable gate array type.

9. (previously presented): An apparatus according to claim 5, wherein said simulator further comprises at least one of:

an analog-to-digital converter which forward digital signals representative of analog signals generated by said unit to said microprocessor, and

a digital-to-analog converter which forwards analog simulation signals based on digital signals generated by said microprocessor to said unit.

10. (currently amended): ~~An~~ The apparatus according to claim ~~5~~6, wherein said at least one ~~of said~~ programmable logic circuit and said at least one second programmable logic circuit is programmed as a function of the type and/or intended use of said unit.

11. (canceled).

12. (new) The method according to claim 1, wherein the duration of the period of the slow output signal is substantially equal to a first plurality of milliseconds and the duration of a period of the fast output signal is substantially equal to a second plurality of microseconds.

13. (new) The method according to claim 1, wherein the first frequency is substantially equal to 1 MHz and the second frequency is substantially comprised between 100 Hz and 100 kHz.

14. (new) The method according to claim 1, wherein the microprocessor has a cycle time substantially equal to ten microseconds.